IN THE CLAIMS:

1. (Withdrawn) A semiconductor device comprising:

a gate electrode formed over a semiconductor region with a gate insulating film interposed therebetween;

an extended high-concentration dopant diffused layer of a first conductivity type that has been formed in part of the semiconductor region beside the gate electrode through diffusion of a first dopant; and

a pocket dopant diffused layer of a second conductivity type that has been formed under the extended high-concentration dopant diffused layer through diffusion of heavy ions,

wherein the pocket dopant diffused layer includes a segregated part that has been formed through segregation of the heavy ions.

2. (Withdrawn) A semiconductor device according to claim 1, wherein the segregated part of the pocket dopant diffused layer overlaps with a profile of the extended high-concentration dopant diffused layer.

3. (Withdrawn) A semiconductor device according to claim 1, further comprising:

a sidewall formed on side faces of the gate electrode; and

a high-concentration dopant diffused layer of the first conductivity type, which has been formed in part of the semiconductor region beside the sidewall to come into contact with an outer periphery of the extended high-concentration dopant diffused layer, has a junction deeper than that of the extended high-concentration dopant diffused layer and has been formed through diffusion of a second dopant.

4. (Withdrawn) A semiconductor device according to claim 1, further comprising a dopant diffused layer, which has been formed in part of the semiconductor region under the gate electrode through diffusion of a third dopant and will be a channel region.

5. (Withdrawn) A semiconductor device according to claim 1, wherein the heavy ions are indium ions.

6. (Currently Amended) A method for fabricating a semiconductor device comprising:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask, thereby forming a first ion implanted layer of a second conductivity, at least upper part of which is an amorphous layer;

a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of a first conductivity type; [[and]]

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming an extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and a pocket dopant diffused layer of the second conductivity type, which is in contact with a bottom portion of the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively[[,]];

<u>implanting ions into a surface part of the semiconductor region, thereby forming a fourth ion implanted layer of a second conductivity type before the first step is performed; and</u>

<u>conducting a third annealing process to activate the fourth ion implanted layer, thereby forming a dopant diffused layer to be a channel region,</u>

wherein in the second step, a dislocation loop layer is formed in the lower region of the amorphous layer in the semiconductor region due to the heavy ions implantation, in the fourth step, the pocket dopant diffused layer is formed having a peak dopant concentration produced by trapping heavy ions in the dislocation loop layer, the pocket dopant diffused layer and the extended high-concentration dopant diffused layer are in contact at the peak dopant concentration of the pocket dopant diffused layer, and a side of the extended high-concentration dopant diffused layer, located below the gate electrode, is not

covered by the pocket dopant diffused layer,

the heavy ions are indium ions, and

an implant dose of the indium ions in the second step is about 1×10^{14} to $1 \times 10^{16}/cm^2$.

7. (Previously presented) A method for fabricating a semiconductor device according to claim 6, wherein the part of the pocket dopant diffused layer in which the heavy ions are trapped overlaps with a dopant profile of the extended high-concentration dopant diffused layer.

8. (Previously Presented) A method for fabricating a semiconductor device according to claim 6, further comprising the steps of:

forming a sidewall spacer on side faces of the gate electrode after the third step has been performed;

implanting ions of a second dopant into the semiconductor region using the gate electrode and the sidewall spacer as a mask, thereby forming a third ion implanted layer of the first conductivity type; and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer of the first conductivity type, which is located outside of the extended high-concentration dopant diffused layer, has a junction deeper than that of the extended high-concentration dopant diffused layer and has been formed through diffusion of a second dopant.

9. (Previously Presented) A method for fabricating a semiconductor device according to claim 8, wherein the heavy ions are implanted at such an implant energy as forming an amorphous/crystalline interface, through implantation of the heavy ions, at a level equal to or deeper than a range of the first dopant and shallower than a range of the second dopant.

10.-11. (Cancelled).

12. (Previously Presented) A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as

making a range of the heavy ions equal to or deeper than a range of the first dopant and between one to three times as deep as the range of the first dopant.

13.-14. (Cancelled)

15. (Original) A method for fabricating a semiconductor device according to claim 6, wherein the first annealing process is a rapid thermal annealing process in which the semiconductor region is heated up to a temperature between 950°C and 1050°C at a rate between 100° per second and 150° per second and then kept at the temperature for a period of time between 1 second and 10 seconds.

16.-20. (Cancelled).

21. (Original) A method for fabricating a semiconductor device according to claim 6, wherein the first dopant is arsenic.

22. (Cancelled)

23. (Previously Presented) A method for fabricating a semiconductor device according to claim 8, wherein the first dopant and the second dopant are arsenic.

24. (Currently Amended) A method for fabricating a semiconductor device according to claim [[10]] 6, wherein the fourth ion implanted layer is formed into the surface part of the semiconductor region by implanting indium ions.